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Author	Subject Category	No. R82EMH002
J. Charles Gioia	Packaging, VLSI/VHSIC, Semiconductors	Date October 1982

Title: A SYNERGISTIC SOLUTION TO THE PROBLEM OF PACKAGING AND INTERCONNECTING VLSI/VHSIC CHIPS

Copies Available at	GE Class 1	No. of Pages
MESO TIS Distribution Center Box 4840 (CSP 4-18) Syracuse, New York 13221	Govt Class Unclassified	30

Summary

Solutions are required for the many problems faced by the chip packaging and interconnection systems industry for effectively meeting the demanding application requirements of the rapidly emerging very-large scale integration/very-high speed integrated circuits (VLSI/VHSIC) chips. Present packaging technologies are being stretched beyond their original concepts thus requiring a new approach to the problem solution. The Military Electronics Systems Operations (MESO) has developed a new packaging approach, based on the Direct Bond Copper Process, which addressed these problems providing a completely integrated system. The problem solution starts at the chip level where en masse connections are made to the chip, chip heat is more effectively managed, low-cost chip hermetic seals accomplished, and then continues providing improved means for interconnecting many VLSI/VHSIC chips.

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SECTION Manufacturing Production Operations

UNIT HIC Facility

MESO ACCOUNTING REFERENCE 442

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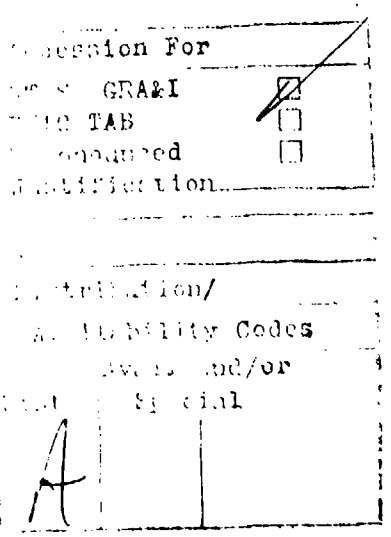
ACKNOWLEDGEMENT

This work has been and continues to be a group effort. We wish to take this opportunity to thank Terry Furhobden (Mgr of the HIC Facility) for his continuous encouragement and support; Joe Cook, Joe Dickson, Don Kortkamp, Betty Phillips, Tom Roseyear and Fran Gantley for the development and implementation of various phases of this program. Of course, without the support of other MESO activities and personnel such as UEPD, Advance Engineering and the MCF Program, very little would have been accomplished to date.



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GLOSSARY

ATR	Airborne Transport Rack
BTAB	Bumped-Tape Automated Bonding
C	Centigrade (Celsius)
CAD	Computer-Aided Design
CAM	Computer-Aided Manufacturing
CCC	Ceramic Chip Carrier
CTE	Coefficient of Thermal Expansion
Cu	Copper
DB	Direct Bond
DIP	Dual In-Line Package
EMSP	Enhanced Modular Signal Processor
ETAS	Escort Towed Array Sonar
HCC	Hermetic Chip Carrier
HIC	Hybrid Integrated Circuit
IC	Integrated Circuit
in.	Inch
I/O	Input/Output
JEDEC	Joint Electronic Device Engineering Council
LSI	Large Scale Integration
MCF	Military Computer Family
MESO	Military Electronic Systems Operations
ML	Multilayer
PCB	Printed Circuit Board
PWB	Printed Wiring Board
RTV	Room Temperature Vulcanizable
SEM	Standard Electronic Module
sq	Square
TAB	Tape Automated Bonding
VHSIC	Very-High Speed Integrated Circuit
VLSI	Very-Large Scale Integration

SECTION I

THE PROBLEM

Solutions are required for the many problems faced by the chip packaging and interconnection systems industry to more effectively meet the demanding application requirements of the rapidly emerging very-large scale integration/very-high speed integrated circuit (VLSI/VHSIC) chip. The problem is discussed in the NAVY report "Analysis of Impact of VHSIC Phase I on the SEM Program" dated 3 November 1981 2271f1266F CRANE TR#. These problems are also well stated in the article by Nathaniel Snyderman entitled "Interconnection Systems - The Unresolved Issues" appearing in the November 23, 1981 issue of Electronic News. The first portion of the article listing the problems is excerpted below:

> Entering a new critical period of development, interconnection systems suppliers are stretching the capabilities of their technology, seeking new ways of attacking emerging problems, and reinvestigating old, discarded approaches.
>
> The neat little chip carrier, embraced when the dual in-line (DIP) package showed signs of outliving its usefulness, is still popular, but is revealing its own limitations.
>
> Interconnect people are considering the pin-grid array approach, such as that developed by IBM in the mid-1960's, as an alternate packaging method for chips with high lead counts. They also are re-evaluating the flatpack, used before the DIP was developed.
>
> Ceramic thick-film hybrid packagers, who were content to work on 1 x 2-in. substrates in the past, are using big circuits loaded with interconnects on 4 x 4-in. substrates and up, in attempts to push sizes up as far as the material permits.
>
> Printed wiring board (PWBs) are getting smaller holes and tighter densities in a drive by the designers to get down to the density of the ceramic.
>
> Each group seems to be reaching for the characteristic of the other, and appears to be heading to a midway point between the ceramic and the PWB.
>
> In Essence, Their Technologies are being stretched to do the things they weren't meant to do.
>
> Propelling these activities is the emergence of new large scale integration (LSI) devices with large lead-counts and the development of VLSI devices in the labs, with their impending application to the production line.
>
> Certainly, each generation of devices has spurred the interconnect suppliers into new development to accommodate them. Now, however, the new devices are revealing some basic interconnect limitations.

Input/output (I/O) terminals must be sharply increased, large area substrates are required, with good heat dissipation properties. The interconnection system must be manufacturable from small prototype orders to large quantities, and be cost-effective in both cases, observers indicate.

No current interconnect system appears able to meet all these requirements. There still are many crucial dilemmas to be resolved.

Complicating the problem is the increasing use of computer-aided design/computer-aided manufacturing (CAD/CAM) approaches to reduce the design time of new circuits from months to weeks and speed up the application of the device to production.

"What's happening today," said Charles Lassen, advanced interconnections manager, PCK Technology, Melville, NY, a part of Kollmorgen's interconnection group, "is that you're seeing design engineers all over the country with chip carriers on their drawing boards, scratching their heads and wondering how they're going to interconnect them."

"How many layers will they use? How will they overcome mismatches in temperature coefficient of expansion? Will they use leadless or leaded carriers? And, because they're substantially increasing heat effects, how will they deal with thermal problems?" (Excerpt ends)

These issues are real and are not simply projections of problems expected to come in the future. These problems began surfacing at GE-MESO about 5 years ago starting with the escort towed array sonar (ETAS) program to the present day enhanced modular signal processor (EMSP) and military computer family (MCF) programs. These programs make extensive use of high-density/high-speed digital circuitry with increasing pressure with time to add the latest VLSI chips. This now drives the need for close spacing of chips to minimize line lengths and reduce signal propagation delays which then dictates dense multilayering for chip interconnects and more severe thermal management problems. Thus, given the pervasiveness of the problem it is felt that a global solution is required. It must start at the chip design and its initial connection to the chip package. In turn the chip package must be responsive to the needs of the next level interconnect/support structure (board level) just as it must meet the needs of the chip.

SECTION II

CHIP PACKAGING BACKGROUND

A brief discussion of three different technologies used for mass terminating semiconductor integrated circuit (IC) chips is presented.

Tape automated bonding (TAB) of IC semiconductor chips has been demonstrated to be a very-reliable low cost means of mounting and wiring chips into first level packages. Its greatest usage during the past 10 years has been at the basic semiconductor wafer producers facilities where high volume products are initially identified for TAB production. Having once identified a chip for TAB assembly, appropriate additional process steps are required at the wafer level to form bumps on the I/O pads on the perimeter of the chip. In some instances, the chip may require a special layout design to accommodate these bumps. Then a copper tape, usually supported on a polymer film, has to be designed to match the bump pattern on the chip for the inner leads. The outer leads of the tape are designed to match the package pads. The machinery for handling TAB production is highly developed and readily adapted for special applications. Thus, this TAB technology readily meets technical and economic criteria for the high-volume basic producer of semiconductors.

The limitation of TAB is that the nonwaffer producer who buys chips in low volume for hybrid application or wafer producers who do not identify high volume uses for the IC cannot justify the additional cost of the process steps required to bump wafers. Therefore, the benefits to be derived from TAB are not achieved for these low volume products. Alternatively, for various reasons, wafers are not readily procurable for the low volume user to do his own customized bumping, even if he were ready to take the risk involved in possible compromising chip performance by doing bump processing separately after wafer completion. Additionally, the increasing complexity of the larger scale ICs (60 plus I/O pads) imposes a severe strain on TAB technology. Inner lead stability of the tape is difficult to maintain in processing, such that it precisely matches the corresponding bump on the chip. Exacerbating the matching problem is the large mismatch of coefficient of expansion of the silicon chip and the copper tape (4-5 times greater than silicon) with its polymer support. This mismatch causes relative movement of the precise inner lead of the copper tape vs the silicon chip as occurs when thermally bonding the lead to the chip. This movement is tolerable with relatively low I/O counts where chip pad sizes can be made relatively large such as 4-mils sq on 7-mil centers. Whereas VLSI chips having 100 plus I/Os will use pads in the order of 2-mil sq on 4-mil centers. These small pads are dictated by the limited availability of chip perimeter where the I/O pads are located for TAB chips.

To overcome the low volume problems related to TAB, the bumped-tape automated bonding (BTAB) concept was developed. This concept differs from TAB by virtue of having the bump formed on the tape rather than on the chip thus obviating the need of bumping the chip, i.e., standard chips or wafers with the usual aluminum I/O pad metallization. Thus, the low volume user has only to invest in the tape tooling ($2-5K) to gain the advantages of TAB without getting into the very specialized business of additionally processing wafers. This BTAB technology has not found wide use, if any, in industry because of difficulty in maintaining planarity of bump tops, hardness of the bumps, and maintaining bump positional accuracy with relation to chip pad locations. (See Brown/Kanz BTAB Ref. 1.) The same problems associated with large count I/O VLSI in TAB are likely to occur with BTAB.

For many years now, IBM has led the technology in "controlled collapse solder bumped chips". This chip termination scheme is similar to TAB except that it does not use tape but does form bumps at the chip I/O pads. The bumps are made of solder with several layers of refractory metal between it and the conventional aluminum I/O pad on the chip. In assembly, the chip is placed face down on the matching pads of the hybrid and heated, causing the solder to melt and attach itself to the hybrid circuit. Since the solder collapses to match the corresponding pad on the hybrid, the planarity concern of BTAB is eliminated. This technique's successful application at IBM and other such high volume users is assured by virtue of having "in-house" silicon wafer design and fabrication capability coupled with the associated hybrid chip assembly method used for chip packaging. Thus, the low volume chip user is precluded from using this approach because of the nonavailability of a full family of solder bumped chips.

IBM has demonstrated that solder bumped chips meet VLSI high-count I/O needs. They have recently released photographs showing a chip with 216 solder bumps mounted on matching hybrid chip carrier. These bumps are easily accommodated since they are not restricted to the perimeter of the chip, i.e., the bump terminations are grid arrayed across the entire active surface face of the chip. This not only provides more real estate for terminations, but also serves as a means of efficiently dissipating heat directly from the junctions (the source of the heat) without the added thermal resistance of the silicon chip thickness. It is claimed that by having a sufficient number of solder bumps, face-down bump mounted, chip junctions can operate cooler than when the chip is more conventionally mounted to its back side with its junction surface face up. Basic objection to the face-down mounting of chips still exists, especially for military electronics, because of the inability to visually inspect the chip I/O pad connections.

The objective of our packaging development activity is to overcome the limitations imposed by the three above-described mass bonding technologies (TAB, BTAB, solder flip chip) using available infrastructure as it may apply to the total program.

SECTION III

GE-MESO SOLUTION

To address the problems raised,work has been done at GE-MESO,to attack this packaging problem on many fronts. Feasibility and some implementation has been demonstrated as the result of our past three years of activity in this area. These solutions begin at the basic chip level on through its packaging to their next printed circuit board (PCB) interconnection level. This is accomplished at the starting chip design level where chip I/O connections may be made at any point on the chip face rather than only at its perimeter. This feature reduces the number of layers of chip top metallization normally required for very dense chips. Additionally, our approach uses a soft compliant copper bump for en masse connections to the chip I/Os. Figure 3-1 shows chip perimeter bumps (inner chip bumps not shown). The beneficial effects of this chip connection technique are many.

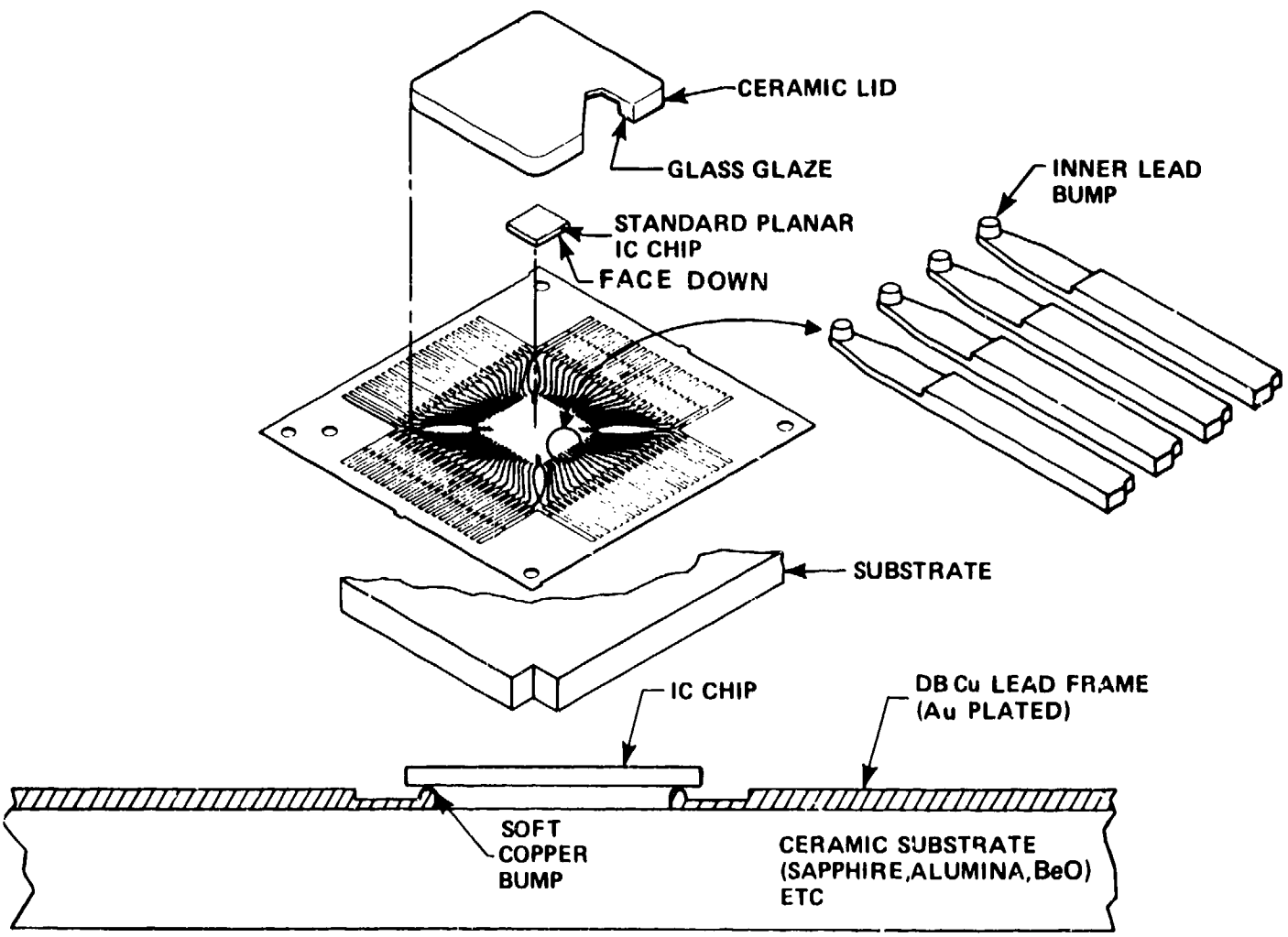

Figure 3-1. DB Cu-Bumped Lead Frame/Slam CCC

3.1 NO REQUIREMENTS FOR SPECIAL METALLIZATION OF CHIP I/O PADS

The copper bumps attached to the face-down mounted chip efficiently conducts heat out of the junction surface (the face being the source of the heat) rather than having to pass through the relatively high thermal impedance of the semiconductor material as would be the case with the more conventionally used backside mountdown of chips. With backside mount down chip designers are driven towards specifying fragile thin chips to reduce thermal impedance. Thus, the ability to efficiently remove heat directly from the points of origin with highly thermal conductive copper (ten-times better than solder bumps) addresses both the thermal management and chip I/O layout concerns facing emerging VLSI/VHSIC products. An important aspect of this program is that it does not require any special metallization of the chip I/O pads; the very conventional planar aluminum metal may be used. The en masse chip connect benefits of this copper bump technology may be achieved with presently available perimeter I/O VLSI chips with more benefits achievable when semicustomized chips are designed with internal I/Os which would make full use of the available features.

3.2 CONVENTIONAL WIRE BONDS NOT USED

Another important aspect of this bump chip attach technology is that conventional wire bonds are not used, being replaced by en masse chip I/O bonds. The cost of making these wire bonds is saved, and in addition the en masse produced bonds are stronger and more reliable. Copper bumps have considerably higher fatigue resistance than solder bumps. Considering the great increase in the number of required I/Os on VLSI/VHSIC, this en masse feature is of significant importance.

This work has some small similarities to the TAB technologies in that it can make use of available slightly modified automated assembly and handling equipments. When this technology is employed with perimeter I/O chips a single-layer copper lead frame having bumps at the ends of the inner leads is intimately direct bonded to a ceramic base to provide precisely positioned firmly held-in-place bumps. As a result of the tight bond of Cu to the

ceramic base, the Cu assumes the same coefficient of thermal expansion (CTE) as the ceramic since the very-ductile Cu readily yields to ceramic. Additionally, the direct bond copper (DB Cu) operation is performed at temperatures in excess of 1065°C making the Cu dead soft. Thus, a number of ideal conditions for bump attachment to chips are attained; (1) the bumps on the tape are very planar and compliantly soft, (2) the Cu tape has the same CTE as the ceramic which now more closely matches that of the silicon chip resulting in less stress imposed on the bump-to-chip bond during thermal excursions, (3) our bump chip bonding work to date using a simple gold flash on the Cu show excellent bond metallurgy resembling that of the widely used thermal compression gold ball wire bond to aluminum pads on chips (Figures 3-2 through 3-5). Other metal systems besides gold plating on the bump and aluminum metallization on the semiconductor chip pads may also be used. Such well-proven metal pair bonding materials may alternatively be used. They are:

1. Gold plate on bumps and gold metallization on chips then thermocompression bonded.

2. Tin plate on bumps and gold metallization on chips for gold/tin low temperature eutectic solder bond.

3. Plain copper bump and aluminum metallization on the chip, then ultrasonically bonded.

Ultrasonic wire bonding of aluminum wires to bare copper is now routinely performed, but to perform this operation en masse on an array of bumps may require thicker silicon semiconductor chips than presently used such that when the ultrasonic energy is transmitted through the chip, it does not crack.

3.3 DB Cu PROCESS ADVANTAGEOUS FOR SAPPHIRE BONDING

The DB Cu process, employed to bond Cu to ceramic, is a mature production process now employed in several plants including the GE-MESO-HIC (hybrid integrated circuit) facility. The process permits the bonding of Cu to a wide assortment of ceramics such as alumina, beryllia and sapphire. The use of sapphire as a lead frame substrate base presents an interesting opportunity to overcome some of the resistance to the use of flip-chip bump bonding because of noninspectability. Sapphire is optically transparent permitting the inspection of the bump bonds to chip pads and also viewing the process as it is being performed.

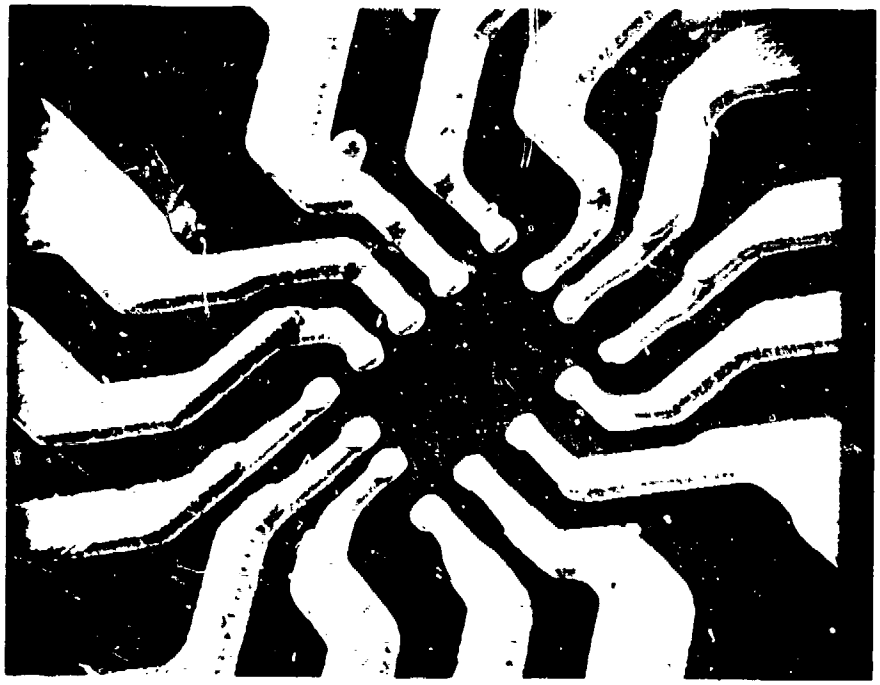

Figure 3-2. Bumped Cu Lead Frame Direct Bonded to Sapphire Base (50 x)

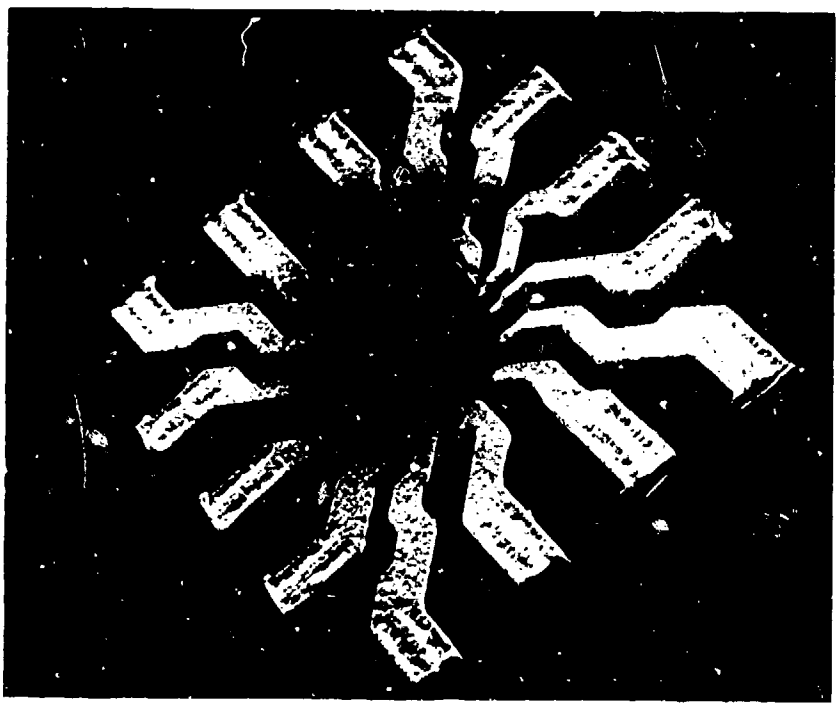

Figure 3-3. Chip Attached to DB Cu Bumped Lead Frame

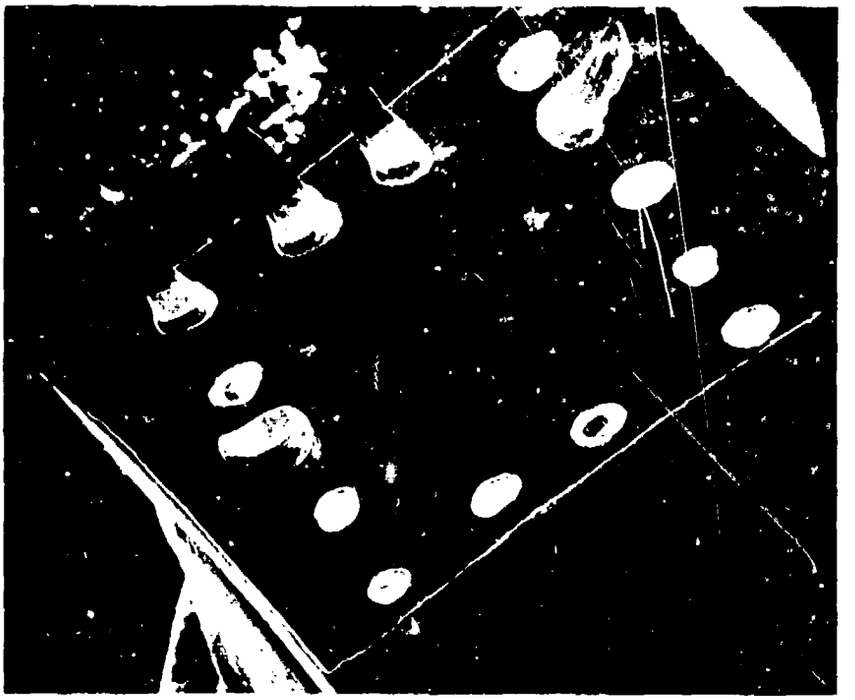

Figure 3-4. Chip Removed from Bumped Lead Frame (Al metal over entire dummy Si chip) Separation through Au (100 x)

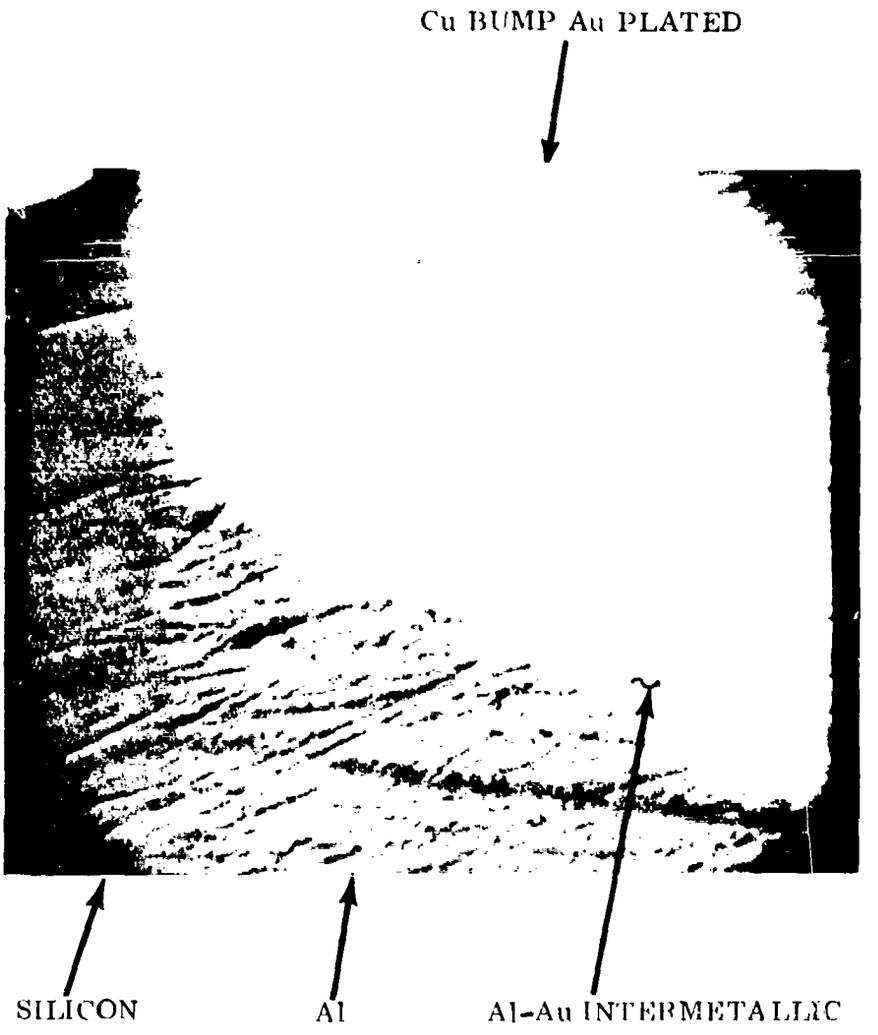

Figure 3-5. Cross Section, Bump Attach to Chip

3.4 DB Cu BUMP ATTACH TO CHIP TECHNOLOGY HAS APPLICATION FOR POWER AND MICROWAVE CHIPS

The DB Cu bump attach to chip technology has application for power and microwave chips as well as digital chips. Figure 3-6 shows how the Cu bumps are applied to a power chip when the emitter, base (E, B, C) connections are on the face of the chip. The Cu leads are designed to accommodate as many bumps as may be required to handle the current and/or heat.

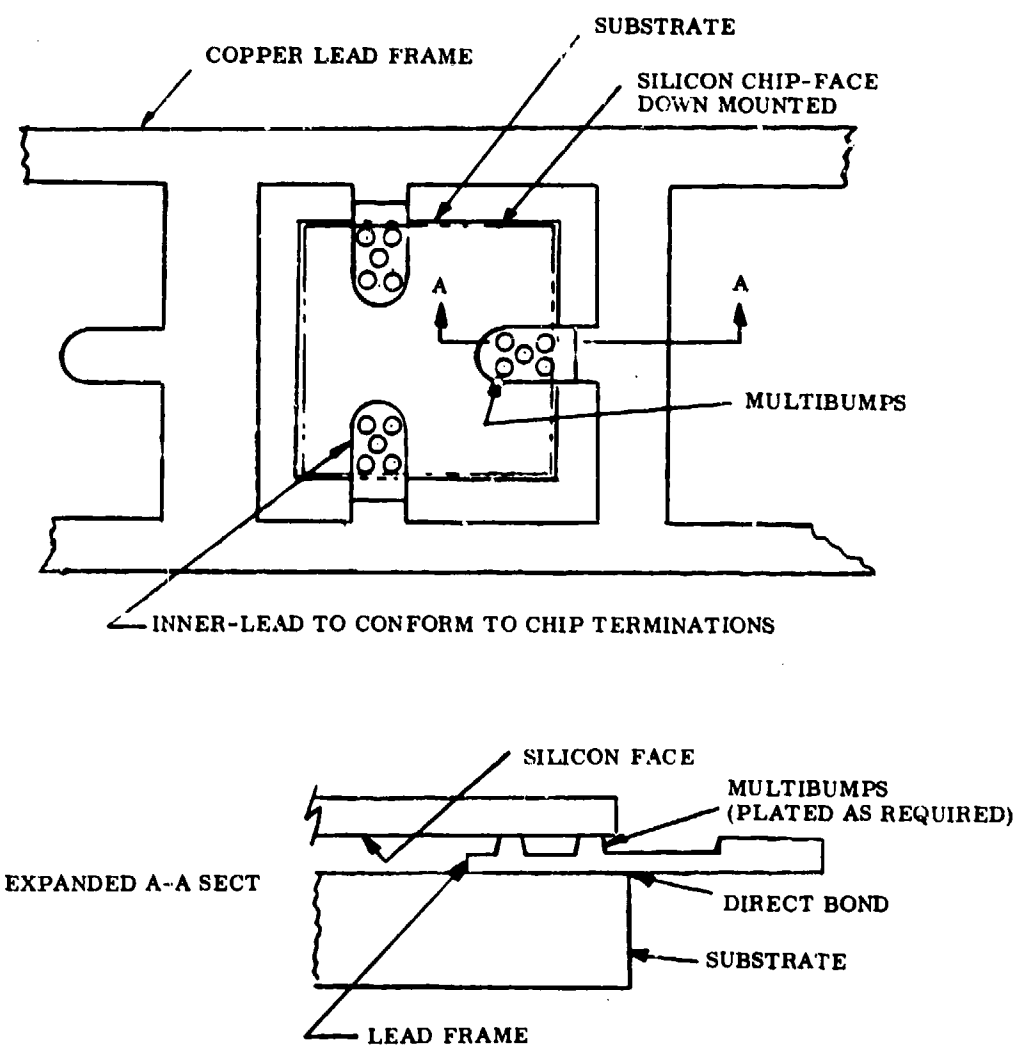

Figure 3-6. High-Power/High-Heat Dissipation DB Cu Application

The opening problem statement covered the problems facing the VLSI/VHSIC packager. We then presented our solution tc the problems relative to the chip level. This included improvements in chip design, thermal management and chip wiring. A broad approach to solving the total VLSI/VHSIC packaging problem has to go beyond the chip level and deal with the next higher levels of packaging. We will describe how the benefits achieved at the chip level are carried through synergistically from the chip hermetic packaging level to the interconnection of many hermetically sealed VLSI/VHSIC chips. The packaging work described below follows Joint Electron Device Engineering Council (JEDEC)chip-carrier dimensional standards but differs in construction technology.

The GE-MESO DB Cu hermetic chip carriers (HCC) uses the same copper lead for mak_ _ both the inner lead connection directly to the chip, and then also becomes the outer flexible lead for the minimum number of connection points and highest reliability (the fewer connection points the greater the reliability). The highly conductive bulk copper lead frame direct bonded to the substrate have outer leads extending beyond the perimeter of the substrate base (see Figure 3-7) which can be formed in many different ways. One mode of forming the outer leads comprises bending them upward (Figures 3-8 and 3-9) away from the base and in a manner which makes them flexible. Then when these leads are connected to a dense multilayer (ML) structure, the concern for matching of the CTE of the ML structure to the ceramic HCC is obviated, the lead flexibility absorbing the mismatch. This flexible outer lead (an integral part of the inner lead) now permits the unencumbered use of a whole family of existing ML structures which may be selected solely on the basis of their most ideal electrical interconnect performance.

Heat emanating from the chip is efficiently managed through the bottom of the ceramic HCC (see Figure 3-10). Heat transfer is facilitated by the use of a relatively thick Cu heat sink intimately direct bonded to the bottom of the ceramic base. Both the lead frame and heat sink are bonded in one operation. Heat now is spread through the copper heat sink base and conductively transferred via an appropriate thermal/mechanical mountdown to a board-level support structure. This support structure has only two simple functions to perform: (1) mechanically support and secure all of the VLSI/VHSIC devices plus other components being interconnected, and (2) optimally transfer heat using simple conduction, heat pipes and convectors as may be required for the cumulative power to be dissipated. Figure 3-11 shows this concept applied to a 2A SEM Form "B" package which has been fabricated and

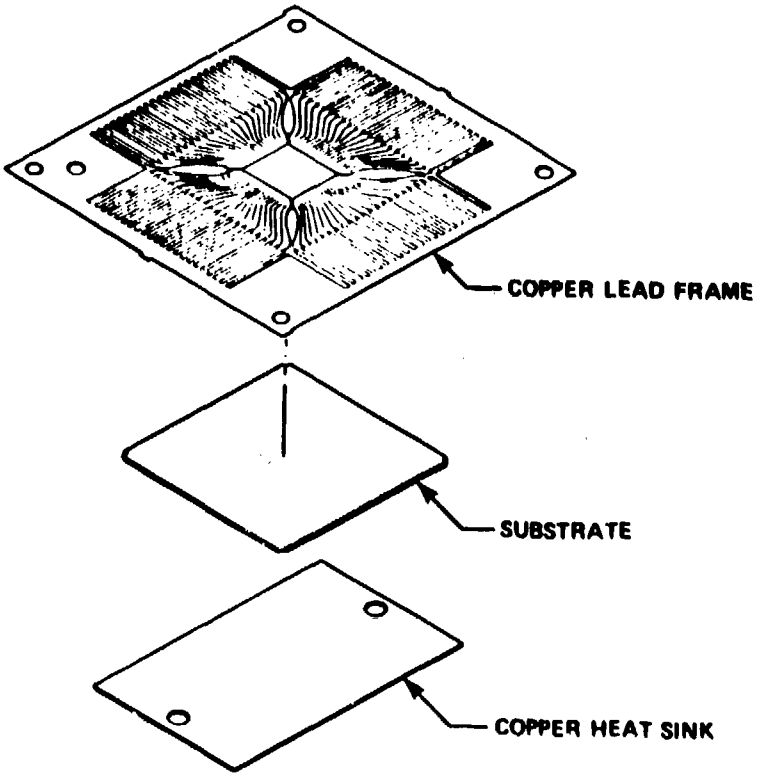

Figure 3-7. DB Cu Lead Frame and Heat Sink to Ceramic Substrate Base

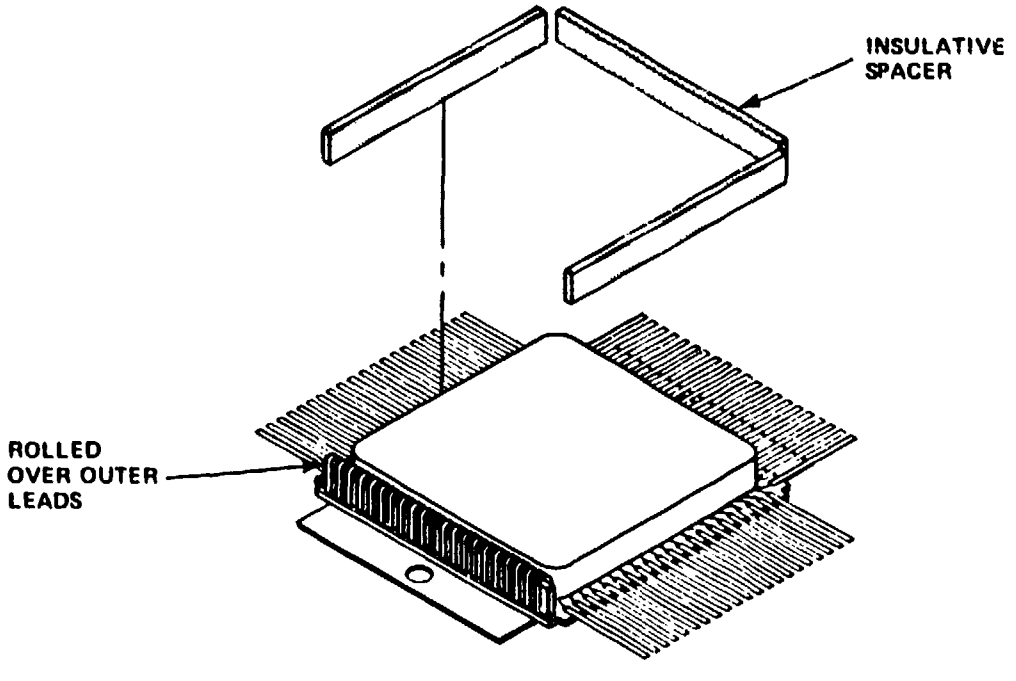

Figure 3-8. Flexible Outer Lead Formation

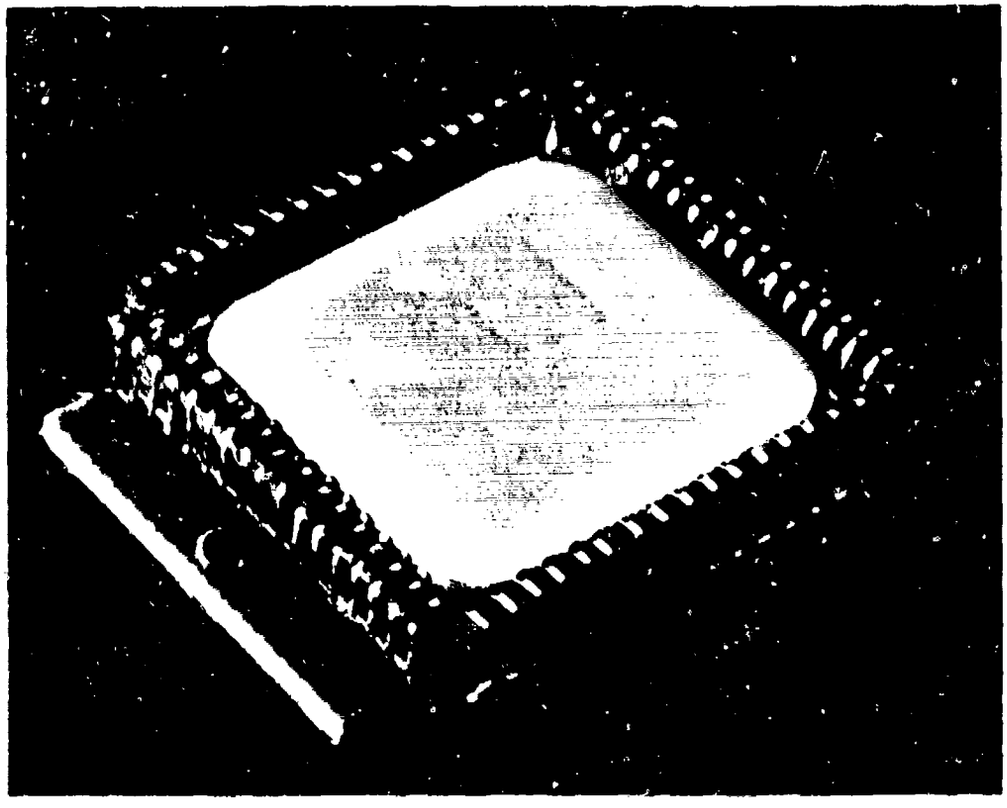

Figure 3-9. Flexibly Leaded HCC with Heat Sink

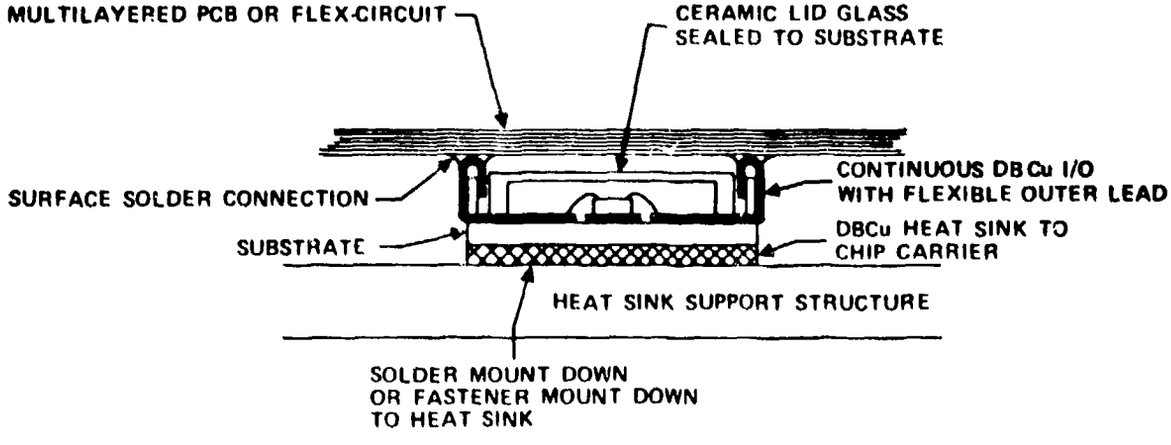

Figure 3-10. Surface Mounted DB Cu Hermetic Chip Carrier (HCC)

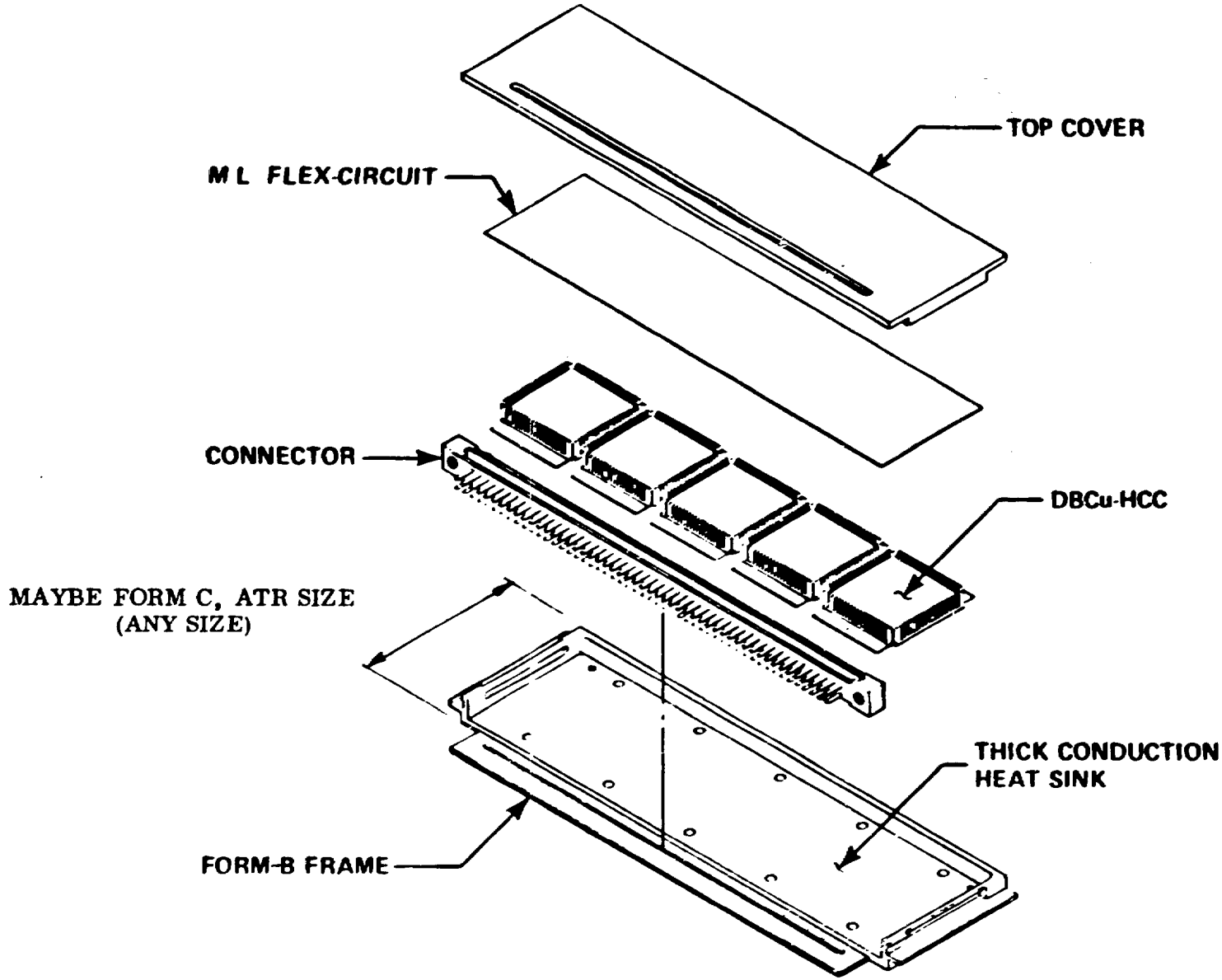

Figure 3-11. HCC-VLSI-2A SEM Form-B Package

shown to have superior thermal performance. Figure 3-12 shows this packaging approach applied to a full ATR size board. Figure 3-13 illustrates how by using ML flexible circuits two-sided interconnected boards may be fabricated.

The virtue of this packaging approach is that the electrical and mechanical/thermal packaging functions are completely separated thereby making it relatively simple to design cost effective and simple means to perform each of the required functions.

We believe that the productive limits have been reached of today's interconnect technology in forcing it to perform these two functions simultaneously. Our packaging approach provides a more rational solution to the problem especially when considering the ever-increasing complexity of each of the problems. An example is electrically interconnecting the many I/Os on numerous VLSI/VHSIC chips when they are densely packaged together and then trying to simultaneously dissipate their increasing heat.

An important part of our work deals with the ability to incorporate the low-cost hermetic glass-sealed ceramic lid process into the DB Cu HCC product. (See Figures 3-14 and 3-15). This hermetic seal process has recently attained a level of maturity in industry which makes it relatively simple to apply to this program. Standard-size ceramic lids are available as catalog items from several vendors together with machinery for making the hermetic glass seals to HCC. This availability plus our long time experience in making hermetic glass seals to copper circuitry assures successful implementation of this process into production.

Considerable versatility is provided by this packaging approach as shown in Figure 3-16 which illustrates other outer lead options.

At this time, HCC vendors offer ceramic carriers with pin-grid array terminations on 0.100-in. centerline spacings. These plugable pin-arrayed packages appear to meet the needs of circuit designers performing their breadboard work where the ability to easily remove and replace packaged chips is important. These arrays may also be used in a more permanent mode when soldered into a PCB. To provide a comparable pin-arrayed package using the DB Cu HCC techniques, we have built several demonstration models showing how this is easily accomplished (see Figure 3-17). There are many advantages to this approach

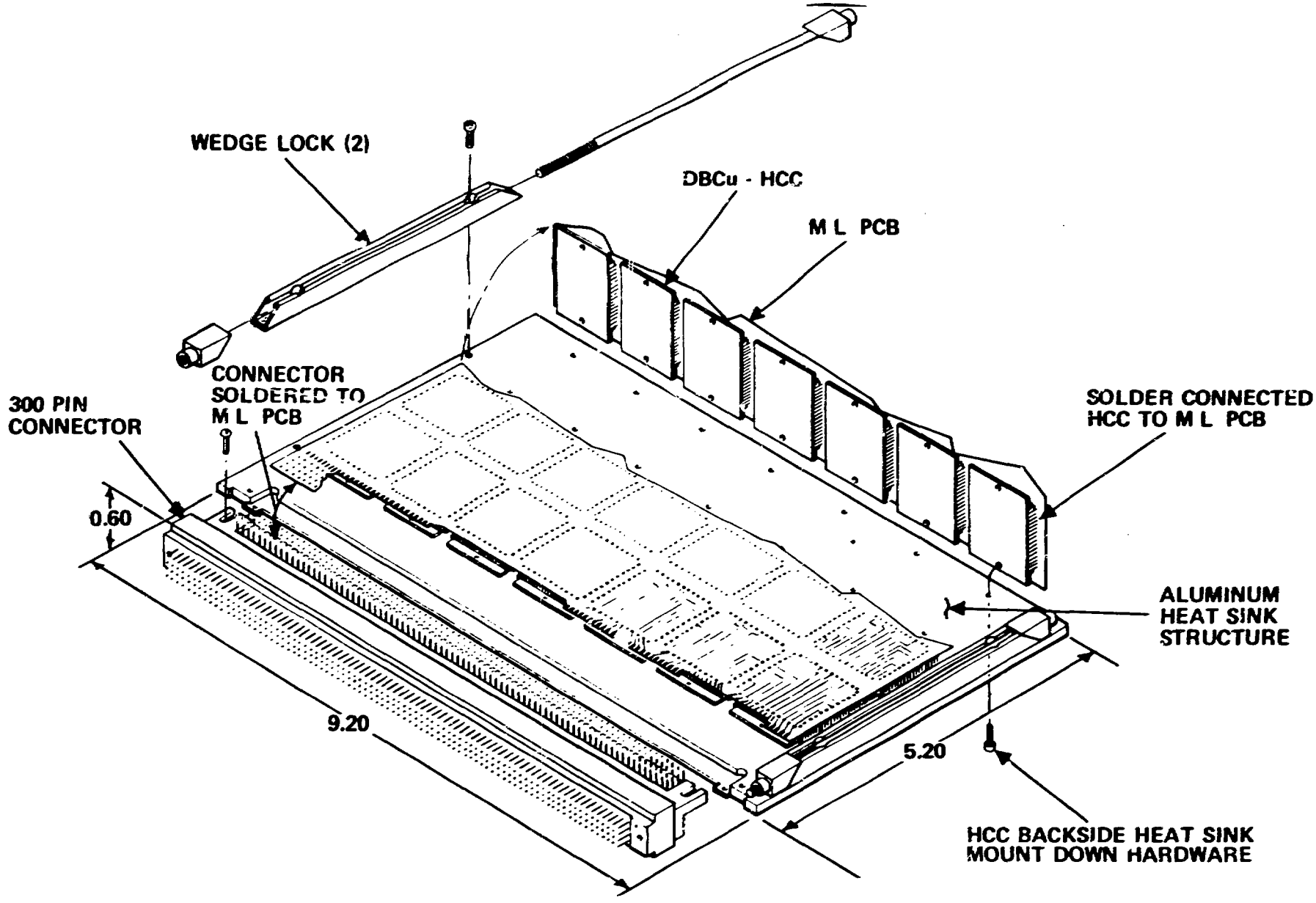

Figure 3-12. Single-Sided Full ATR (Interconnect PCB Separated from Heat Sink Structure)

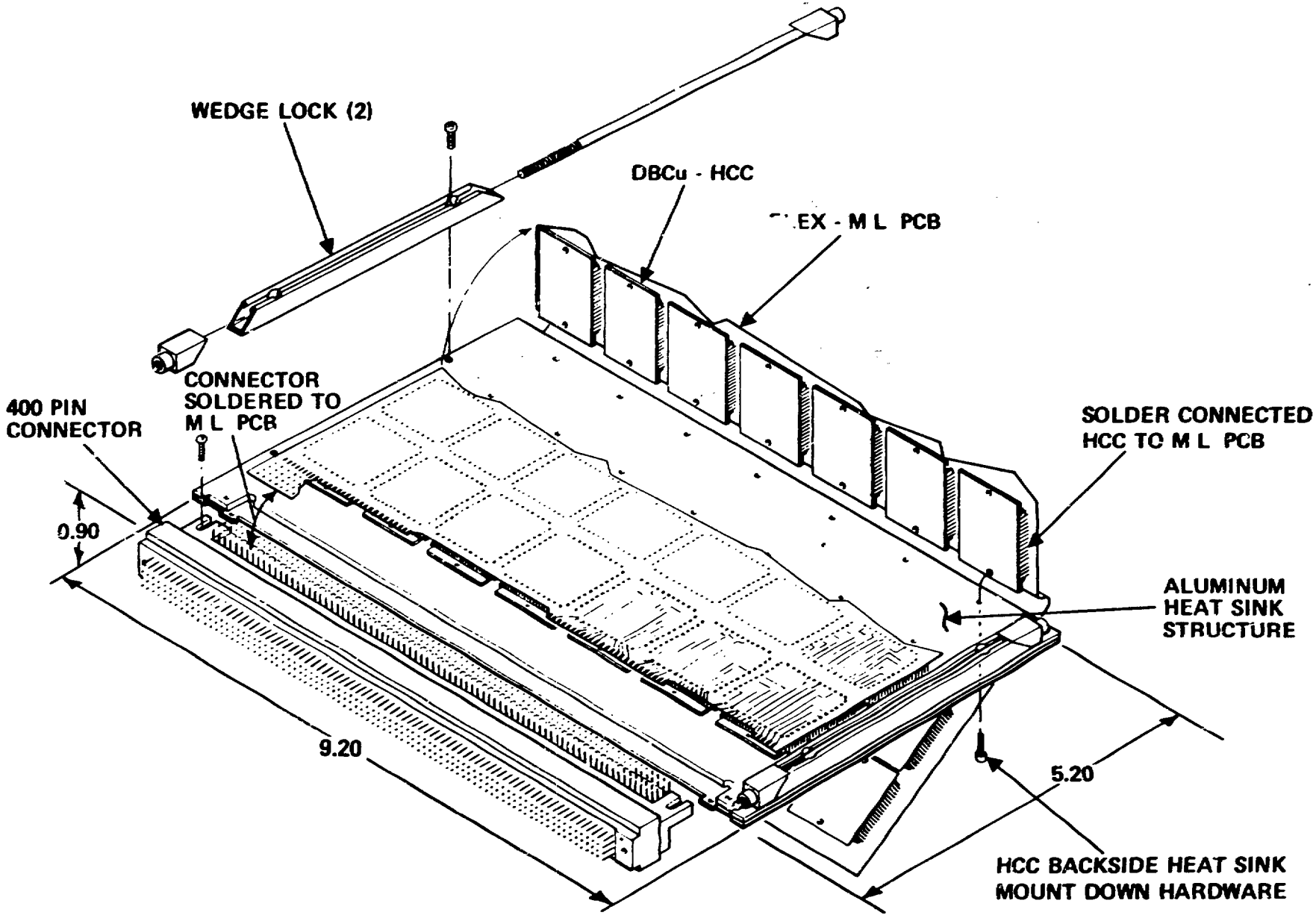

Figure 3-13. Two-Sided Full ATR (Interconnect PCB Separated from Heat Sink Structure)

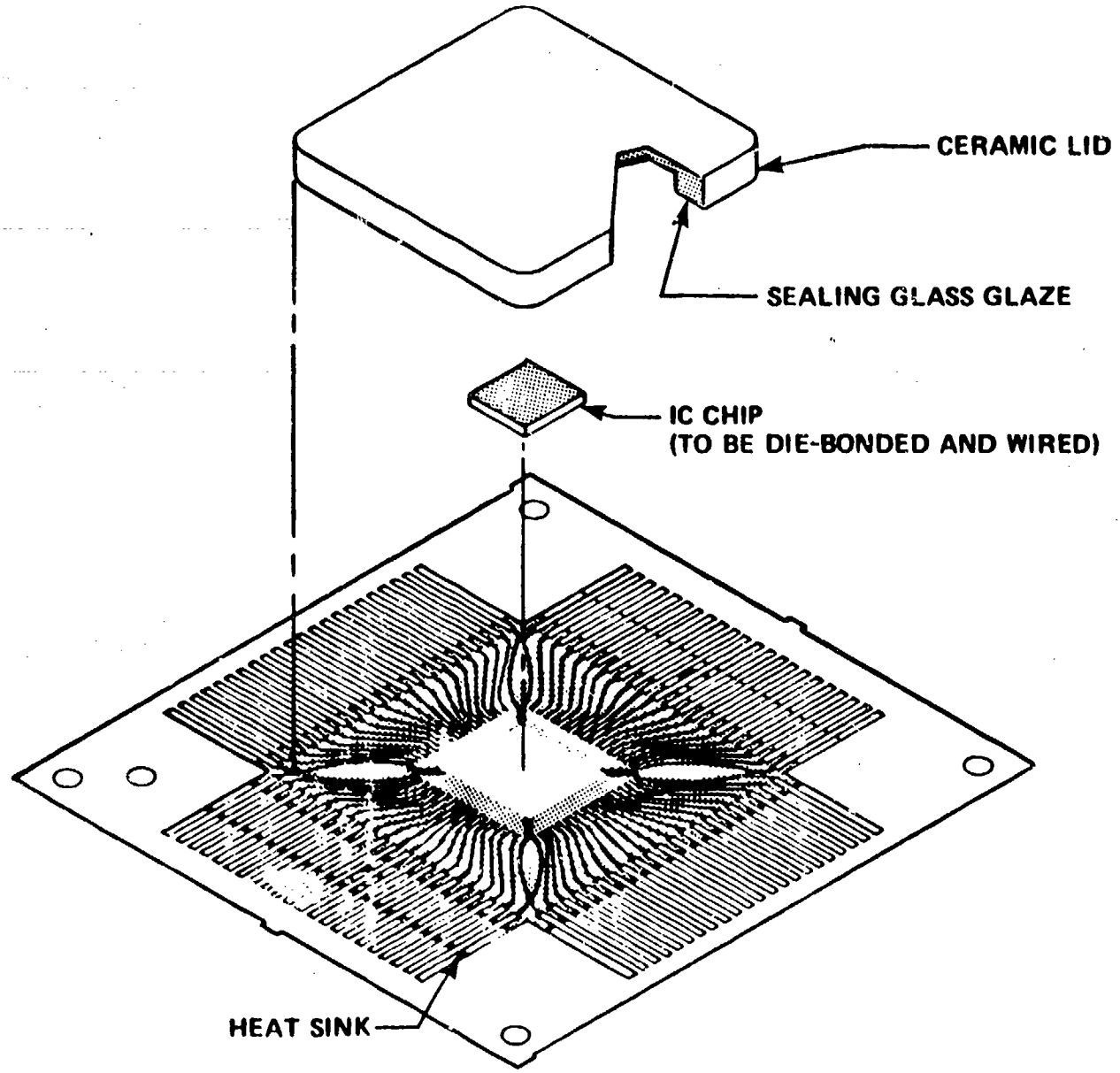

Figure 3-14. DB Cu HCC Assembly and Hermetic Glass Seal

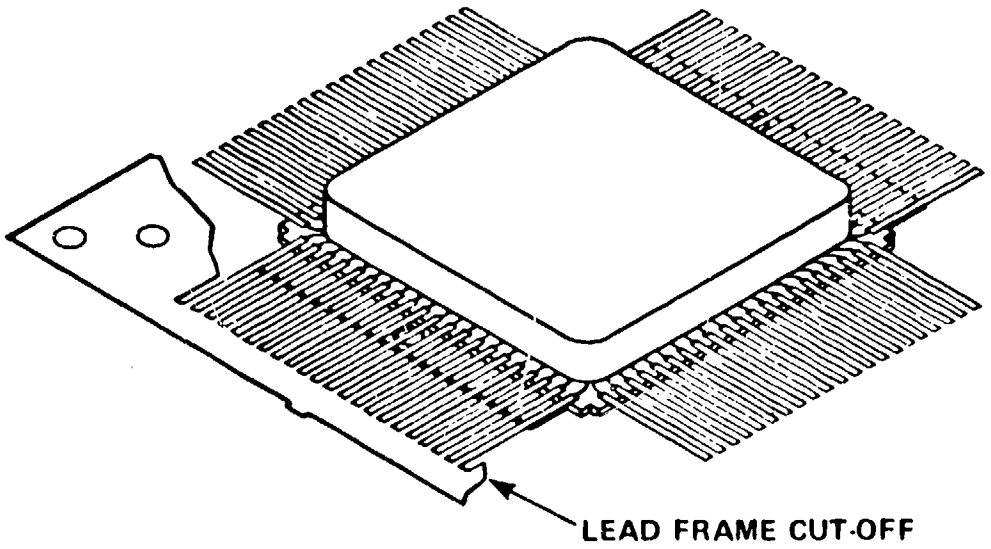

Figure 3-15. Sealed HCC with Outer Leads Excised

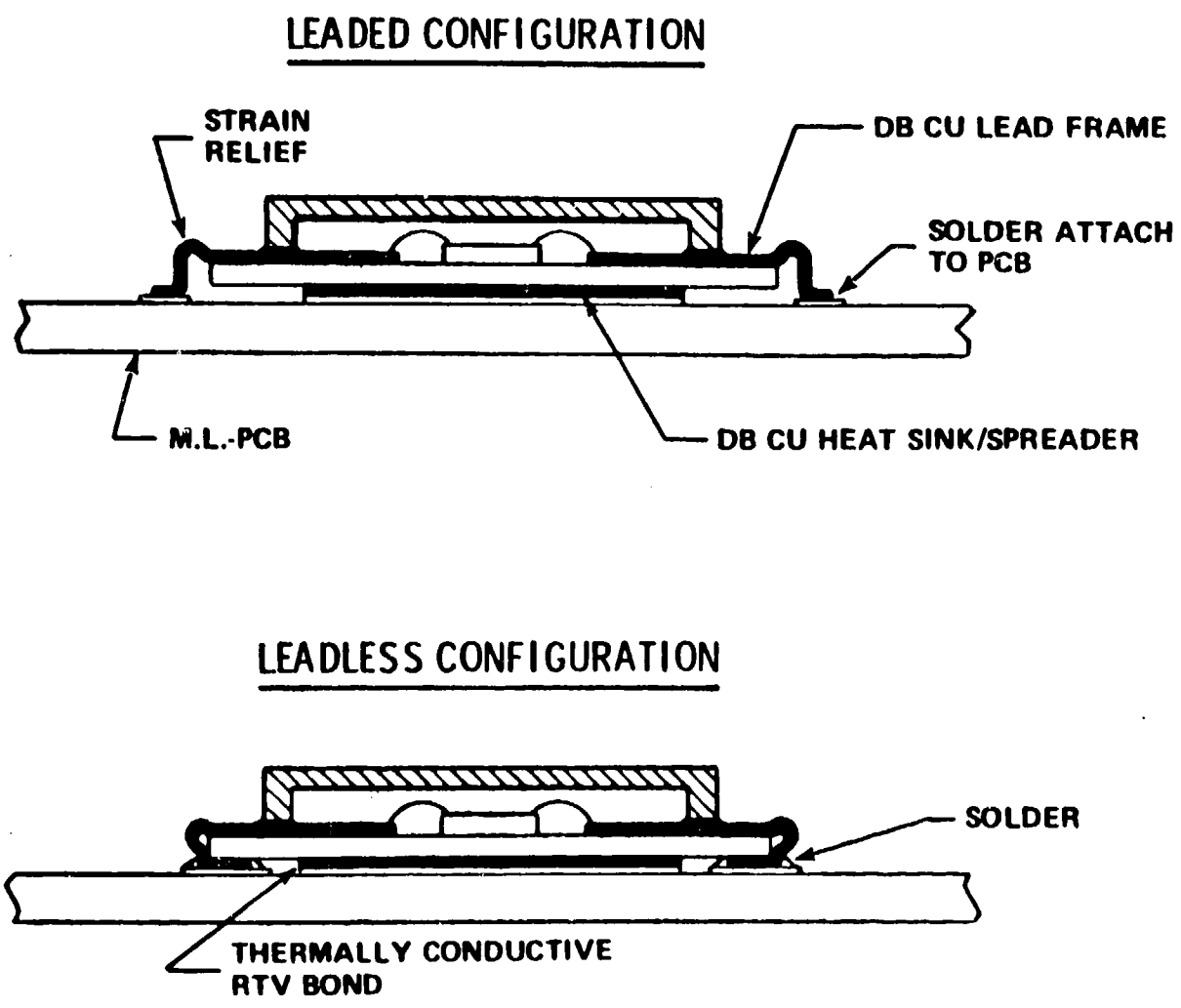

Figure 3-16. DB Cu Chip Carrier with Strain Relief for Direct Mounting to Conventional ML-PCBs

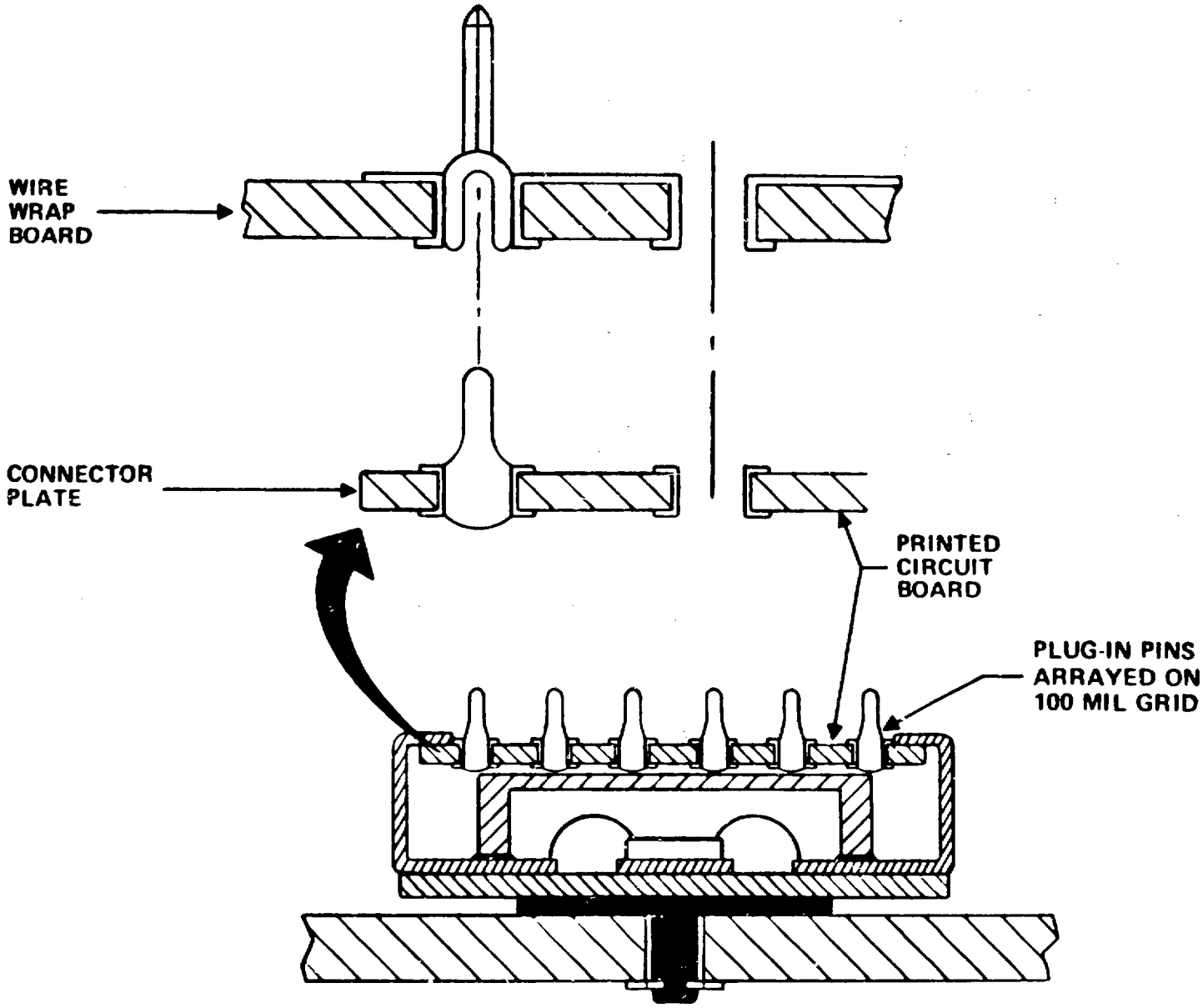

Figure 3-17. Pin Grid Array Application of DB Cu - HCC, Shown as a Plug-in Package into a Wire-Wrap Board

compared to the available pin-arrayed ceramic HCC products. These advantages are enumerated below:

1. Our pin grid array is applied to a separate PCB using standard PCB fabrication methods. As such, they are easily customized to match any existing interconnect PCB grid requirement. This feature is important because of the need to mix HCC packaged VLSI/VHSIC chips with other "today's art" chips which are generally packaged in DIP format. The equivalent ceramic HCCs are made up of multilayer co-fired green tape with refractory metallization and as such, require costly tooling with long lead times. This limits the opportunity to customize and may inhibit the use of VLSI/VHSIC chips.

2. The CTE of our pin-grid PCB exactly matches that of the interconnect PCB, thus eliminating temperature cycle stresses at the many pin solder joints. Our design approach provides for the stress to be relieved through the flexible DB Cu outer leads. This problem will become more severe as the ceramic HCC becomes larger to accommodate high pin count chips.

3. We provide, in our design, a very optimal means for dissipating heat from the chip while at the same time providing maximum density of pins. For 100 or more pins the pin grid array ceramic HCC package has the chip mounted on the same side of the package as the pins. Essentially no conduction heat path is provided, whereas in our concept the chip is always mounted on the side opposite the pins for thermally efficient attachment to the heat sink. As stated earlier and also applicable here, the interconnect wiring is isolated or separated from the mechanical/thermal function. This can be a powerful feature in diminishing the lead time required to develop a systems functional block. The mechanical engineer in parallel with the circuit designer can design the "black box" to accommodate the thermal load and mechanical support structure. At the same time, the circuit designer can be breadboarding and debugging his circuit using a heat sink structure which is close to the final design, if not the final design. The present scenario has the circuit designer breadboarding on an oversized board to accommodate HCC connectors, with inadequate cooling for his chips, and long lines for the interconnect of the chips. All of these factors, especially for high speed circuits, produce erroneous results, thus causing another full circuit development iteration when the final packaging form evolves.

SECTION IV

STATUS AND SUMMARY

Demonstration hardware embodying all of the facets of the GE-MESO VLSI/VHSIC packaging developments have been built. Some DB Cu HCC packages with 109 pin-grid array terminations have been built for use in packaging gate array IC chips on a military computer now under development. Initial environmental testing on all of the subject packaging developments has also been performed. All more than adequately demonstrated the soundness of the packaging approach. Considerable work has yet to be performed to verify the producibility, reliability, and cost effectiveness of all aspects of this packaging program. Our current plan to accomplish the objectives of this program separates the program into two parts; one deals only with the en masse DB Cu bump attachment to the chips and the other dealing with the DB Cu HCC and its next level assembly. DB Cu flexibly leaded HCC need not use the DB Cu bump chip attach process using instead present art automatic wire bonding machinery.

The goal of the GE-MESO VLSI/VHSIC packaging development work has been to provide a complete integrated approach to the problem solution. We have demonstrated feasibility showing the synergistic relationship and value of combining all the facets of our work. Starting at chip design and its I/O wiring, we provide improved means to get the heat out of the chip and means to efficiently provide for a large number of I/Os. The heat then is readily transferred through low thermal resistance copper bumps into its integral copper base heat sink for attachment to the PCB level assembly. Then separately, the PCB level wiring assembly of many VLSI/VHSIC chip is readily handled on the top side of the DB Cu HCC using their flexible leads to accommodate a variety of ML techniques. The total effect of combining all the elements of our proposal is that heat is more efficiently transferred from the chip junction source of heat to cabinet level for low-cost highly reliable system operation. Solid copper electrical connections are made directly to the chip and carried out of the HCC to outer flexible leads without any intervening connection points. These outer leads can be optionally formed in many different modes to match any selected ideal dense ML structure to meet all of the stringent electrical requirements. No compromising of ML structure selection is required to accommodate component support, thermal dissipation and physical size needs.

SECTION V

REFERENCES

1. Brown and Kanz, "BTAB--The Elusive Success", 1980 ISHM Proceedings.

2. Bernard T. Clark, "Designing the Thermal Conduction Module for the IBM 3081 Process", 31st ECC Atlanta, GA, May 11, 1981.

3. Vernon and Vidano, "Manufacturing Technology for Low-Cost Hermetic Chip-Carrier Packaging", T.I. Corp, AFML Contract No. F33615-78-C-5147.

ENGLISH-METRIC/METRIC-ENGLISH CONVERSION TABLE

mm	=	0.1 cm
cm	=	0.3937 in.
cm	=	0.0328 ft
cm	=	10 mm
cm^2	=	0.1550 $in.^2$
cm^2	=	$1.076 \cdot 10^{-3}$ ft^2
cm^3	=	0.061 $in.^3$
cm^3	=	$3.531 \cdot 10^{-5}$ ft^3
ft	=	30.48 cm
ft	=	0.3048 m
ft^2	=	0.0929 m^2
ft^2	=	929.37 cm^2
ft^2	=	$9.294 \cdot 10^{-3}$ km^2
ft^3	=	0.0283 m^3
in.	=	2.54 cm
$in.^2$	=	6.452 cm^2
$in.^3$	=	16.387 cm^2
μm (micron)	=	0.001 mm
μm	=	10^{-6}m
μm	=	10^{-4} cm
μin.	=	$2.54 \cdot 10^{-5}$mm
kg	=	2.2046 lbs
km	=	3281 ft
km	=	0.6214 mi
km	=	0.55 nmi
km^2	=	$1.076 \cdot 10^7$ ft^2
km^2	=	0.381 mi^2
km/h	=	0.913 ft/s
knot	=	1.152 mi/h
oz	=	28.35 g
oz	=	0.062 lbs
lb	=	453.6 g
lb	=	0.4536 kg
metric ton	=	1.12 tons (U.S.)
m	=	39.37 in.
m	=	3.281 ft
m	=	1.0936 yd
m^2	=	10.76 ft^2
m^2	=	1.196 yd^2
m^3	=	35.32 ft^3
m^3	=	1.430 yd^3
mi	=	1.6093 km
mi	=	5280 ft
mi	=	0.87 nmi
mi	=	1760 yd
mi^2	=	2.59 km^2
mi/h	=	0.87 knots
nmi	=	1.852 km
nmi	=	6076 ft
nmi	=	1.15 mi
yd	=	0.9144 m
yd^2	=	0.836 m^2
yd^3	=	0.7645 m^3
qt	=	0.946 liter
liter	=	1.057 qt
acre	=	43,560 ft^2
acre	=	4046.72 m^2
rad	=	57.2958°
deg	=	0.017 rad
°F	=	9/5(°C) + 32
°C	=	5/9(F° - 32)